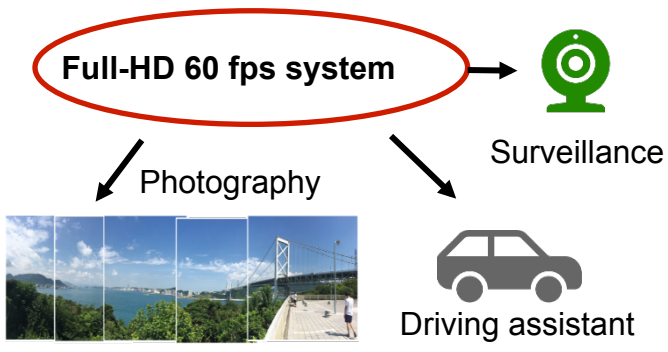
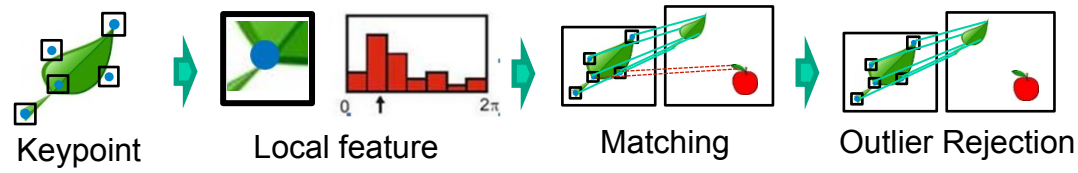
Region-quantified ORB and FIFO-bridge pipelined RANSAC based FPGA Implementation of Robust Full-HD 60fps Matching

修士課程卒業 饒天珉

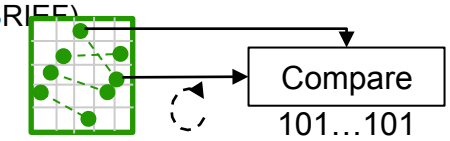
Research background



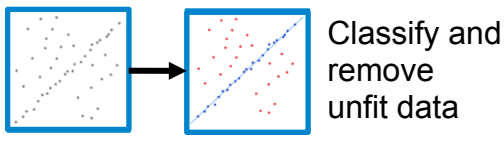
Basic flow 0f local feature based matching



ORB (Oriented FAST and Rotated BRIEF)



RANSAC (Random sample consensus)



Research target

FPGA implementation for Fulll-HD 60fps matching based on ORB feature and RANSAC

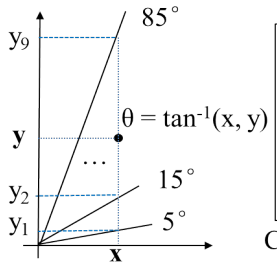
Problems

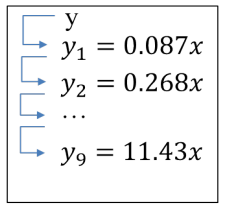
- Non-linear process for orientation
- Sequential in feature generation
- Iteration process in RANSAC

Proposed method

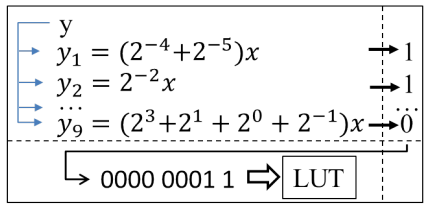
Region quantified ORB

P1: Approximate for arctan() by quantified region



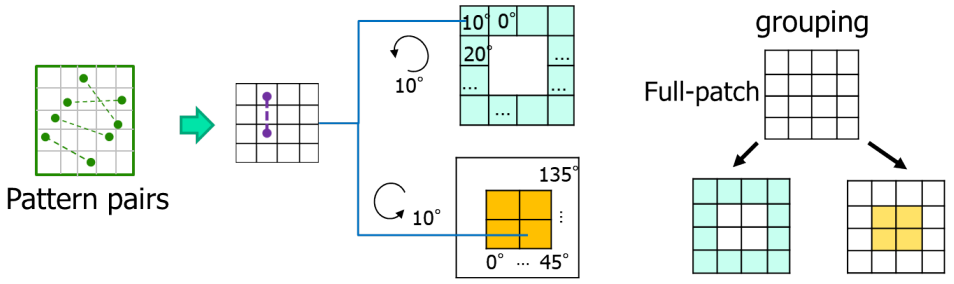


Conventional method



Proposed method

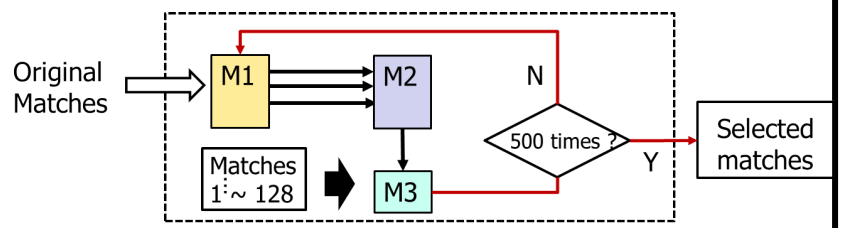
P2: Parallel feature generation by sub-patch grouping



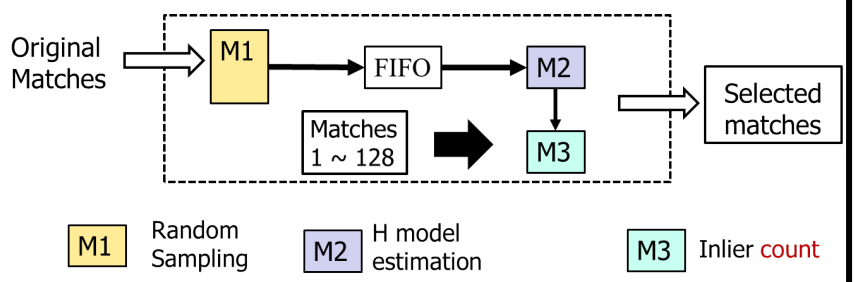
Pipelined RANSAC

P3: Pipelined RANSAC with FIFO-bridge

◆ Conventional structure

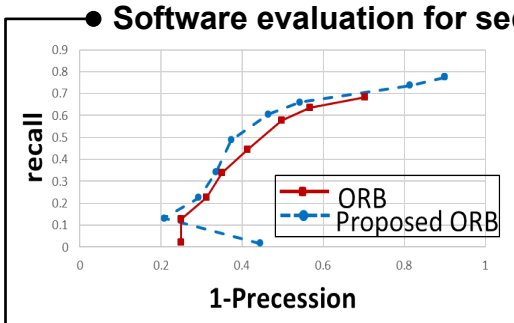


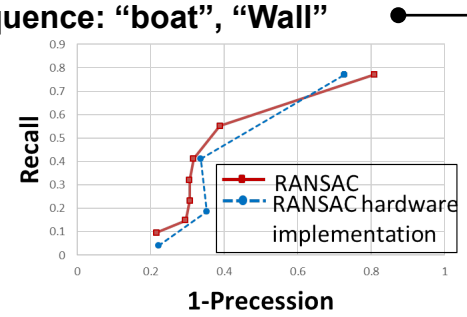
◆ Proposed pipeline structure



Experiment result

Software evaluation for sequence: “boat”, “Wall”





Hardware performance

	Proposed ORB
Max frequency (MHz)	150.121
Image Resolution	Full-HD
Frame rate[fps]	60
Processing time / frame (ms)	13.518

Hard resource cost

	Used	Available	Utilization
# of slice registers	3,0417	94,8480	3%
# of slice LUTs	10,4570	47,4240	22%
# of fully used LUT-FF pairs	1,5751	11,9236	13%
# of Block RAM/FIFO	6	720	0.8%
# of DSP48E1s	786	864	90%

Conclusion:

- Achieve 13.518ms for Full-HD 60 fps matching with RANSAC, and robust to rotation and view point change within certain range.

Graduate School of Information, Production and Systems
Waseda University